IN THE CLAIMS:

Please amend the following claims having the same number as indicated:

1. (Original). A controller, comprising:

a primary processing unit;

a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary and secondary processing units are adapted to run the control algorithm; and,

a functional compare module coupled to the primary processing unit and the secondary processing unit for comparing a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units.

2. (Original). A controller, as set forth in claim 1, wherein the functional compare module is adapted to detect a fault if the primary output and the secondary output are not the same.

3. (Original). A controller, as set forth in claim 1, wherein the primary output and the secondary output are data.

4. (Original). A controller, as set forth in claim 1, wherein the primary output and the secondary output are control signals.

5. (Original). A controller, as set forth in claim 1, wherein the functional compare module is adapted to perform diagnostics upon startup of the controller.

6. (Original). A controller, as set forth in claim 1, including at least one peripheral module coupled to the primary processing unit, wherein the at least one peripheral nodule includes a built in self test circuit for detecting faults within the peripheral module, the built in self test circuit being coupled to the primary processing unit.

7. (Original). A controller, as set forth in claim 1, including at least one bus, wherein the common memory, primary and secondary processing units, and functional compare module are coupled to the at least one bus, wherein the functional compare module is adapted to read signals on the at least one bus, generate a signature of the signals, compare the generated signature with a reference signal and detect a fault if the signals are not the same.

8. (Original). A controller, as set forth in claim 7, wherein the at least one bus includes an address bus, a data bus, and a control bus.

9. (Original). A controller, as set forth in claim 1, wherein the primary processing unit is coupled to a system for control of the system, and wherein the secondary processing unit is adapted to control the system if a fault is detected in the primary processing unit.

10. (Original). A controller, as set forth in claim 9, wherein the secondary processing unit is coupled to a second system for control of the second system.

11. (Original). A method for detecting a fault in a controller, the controller including a primary processing unit, a secondary processing unit coupled to the primary processing unit, and a common memory coupled to the secondary and primary processing units, including the steps of:

reading a control algorithm stored in the common memory by the primary processing unit;

reading the control algorithm stored in the common memory by the secondary processing unit;

comparing a primary output of the primary processing unit and a secondary output of the secondary processing unit and responsively detecting a fault.

12. (Original). A method, as set forth in claim 11, wherein the primary output and the secondary output are data.

13. (Original). A method, as set forth in claim 11, wherein the primary output and the secondary output are control signals.

14. (Original). A method, as set forth in claim 11, including the step of performing diagnostics upon startup of the controller.

15. (Original). A method, as set forth in claim 11, wherein the controller includes at least one peripheral module coupled to the primary processing unit, the method including the step of detecting faults within the peripheral module using a built in self test circuit coupled to the primary processing unit.

16. (Original). A method, as set forth in claim 11, wherein the controller includes at least one bus, wherein the common memory, primary and secondary processing units, and functional compare module are coupled to the at least one bus, and including the steps of:

reading signals on the at least one bus;

generating a signature of the signals;

comparing the generated signature with a reference signal; and,

detecting a fault if the signals are not the same.

17. (Original). A method, as set forth in claim 16, wherein the at least one bus includes an address bus, a data bus, and a control bus.

18. (Original). A method, as set forth in claim 11, wherein the primary processing unit is coupled to a system for control of the system, the method including the step of controlling the system by the secondary processing unit if a fault is detected in the primary processing unit.

19. (Original). A method, as set forth in claim 18, wherein the secondary processing unit is coupled to a second system for control of the second system.

20. (Original). An apparatus for controlling a first system of a motor vehicle, comprising:

a primary processing unit for performing a first set of functions with respect to the first system;

a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary and secondary processing units are adapted to run the control algorithm; and,

a functional compare module coupled to the primary processing unit and the secondary processing unit for comparing a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units.

21. (Original). An apparatus, as set forth in claim 20, wherein the first system is a brake system.

22. (Original). An apparatus, as set forth in claim 20, wherein the first system is a steering system.

23. (Original). An apparatus, as set forth in claim 22, wherein the steering system is a steer by wire system.

24. (Original). An apparatus, as set forth in claim 20, wherein the first system is an engine control system.

25. (Original). An apparatus, as set forth in claim 20, wherein the functional compare module is adapted to detect a fault if the primary output and the secondary output are not the same.

26. (Original). An apparatus, as set forth in claim 20, wherein the primary output and the secondary output are data.

27. (Original). An apparatus, as set forth in claim 20, wherein the primary output and the secondary output are control signals.

28. (Original). An apparatus, as set forth in claim 20, wherein the functional compare module is adapted to perform diagnostics upon startup of the apparatus.

29. (Original). An apparatus, as set forth in claim 20, including at least one peripheral module coupled to the primary processing unit, wherein the at least one peripheral nodule includes a built in self test circuit for detecting faults within the peripheral module, the built in self test circuit being coupled to the primary processing unit.

30. (Original). An apparatus, as set forth in claim 20, including at least one bus, wherein the common memory, primary and secondary processing units, and functional compare module are coupled to the at least one bus, wherein the functional compare module is adapted to read signals on the at least one bus, generate a signature of the signals, compare the generated signature with a reference signal and detect a fault if the signals are not the same.

31. (Original). An apparatus, as set forth in claim 30, wherein the at least one bus includes an address bus, a data bus, and a control bus.

32. (Original). An apparatus, as set forth in claim 20, wherein the secondary processing unit is adapted to control the first system if a fault is detected in the primary processing unit.

33. (Original). An apparatus, as set forth in claim 32, wherein the secondary processing unit is coupled to a second system for control of the second system.

34. (Original). A method for detecting a fault in a controller for use in a motor vehicle, the controller including a primary processing unit, a secondary processing unit coupled to the primary processing unit, and a common memory coupled to the secondary and primary processing units, including the steps of:

reading a control algorithm stored in the common memory by the primary processing unit;

reading the control algorithm stored in the common memory source by the secondary processing unit;

comparing a primary output of the primary processing unit and a secondary output of the secondary processing unit and responsively detecting a fault.

35. (Currently Amended). A method, as set forth in claim 34, wherein the primary processing unit controls ~~first system is~~ a brake system.

36. (Currently Amended). A method, as set forth in claim 34, wherein the primary processing unit controls ~~first system is~~ a steering system.

37. (Currently Amended). A method, as set forth in claim 36 ~~35~~, wherein the steering system is a steer by wire system.

38~~36~~. (Currently Amended). A method, as set forth in claim 34, wherein the primary processing unit controls ~~first system is~~ an engine control system.

39~~37~~. (Currently Amended). A method, as set forth in claim 34, wherein the primary output and the secondary output are data.

40~~38~~. (Currently Amended). A method, as set forth in claim 34, wherein the primary output and the secondary output are control signals.

41~~39~~. (Currently Amended). A method, as set forth in claim 34, including the step of performing diagnostics upon startup of the controller.

42~~40~~. (Currently Amended). A method, as set forth in claim 34, wherein the controller includes at least one peripheral module coupled to the primary processing unit, the method including the step of detecting faults within the peripheral module using a built in self test circuit coupled to the primary processing unit.

43~~41~~. (Currently Amended). A method, as set forth in claim 34, wherein the controller includes at least one bus, wherein the common memory, primary and secondary processing units, and functional compare module are coupled to the at least one bus, and including the steps of:

reading signals on the at least one bus;

generating a signature of the signals;

comparing the generated signature with a reference signal; and,

detecting a fault if the signals are not the same.

44~~42~~. (Currently Amended). A method, as set forth in claim 43 ~~41~~, wherein the at least one bus includes an address bus, a data bus, and a control bus.

45~~43~~. (Currently Amended). A method, as set forth in claim 34, wherein the primary processing unit is coupled to a system for control of the system, the method including the step of controlling the system by the secondary processing unit if a fault is detected in the primary processing unit.

4644. (Currently Amended). A method, as set forth in claim 45 ~~43~~, wherein the secondary processing unit is coupled to a second system for control of the second system.

4745. (Currently Amended). A controller for a motor vehicle, comprising:

a primary processing unit coupled to the motor vehicle and adapted to perform a first set of functions;

a secondary processing unit coupled to the motor vehicle and to the primary processing unit and adapted to perform a set of primary test functions;

a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary processing unit is adapted to run the control algorithm; and,

a functional compare module coupled to the primary processing unit and the secondary processing unit for comparing a primary output of the primary processing unit after the control algorithm has been run and a test output of the secondary processing units and to responsively detect a fault in the primary processing unit, wherein the secondary processing unit is adapted to perform the first set of functions upon detection of a fault in the primary processing unit.

4846. (Currently Amended). A controller, as set forth in claim 47 ~~45~~, wherein the primary processing unit controls ~~first system is~~ a brake system.

4947. (Currently Amended). A controller, as set forth in claim 47 ~~45~~, wherein the primary processing unit controls ~~first system is~~ a steering system.

5048. (Currently Amended). A controller, as set forth in claim 49 ~~46~~, wherein the steering system is a steer by wire system.

5149. (Currently Amended). A controller, as set forth in claim 47 ~~45~~, wherein the primary processing unit controls ~~first system is~~ an engine control system.

5250. (Currently Amended). A controller, as set forth in claim 47 ~~45~~, wherein the secondary processing unit is adapted to perform a second set of functions, and wherein the primary processing unit is adapted to perform a set of secondary test functions, and wherein the functional compare module is adapted to detect a fault in the secondary processing unit, wherein the primary processing unit is adapted to perform the second set of functions upon detection of a fault in the secondary processing unit.

5351. (Currently Amended). A method for detecting a fault in a controller for use in a motor vehicle, the controller including a primary processing unit coupled to the motor vehicle and adapted to perform a first set of functions and a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary processing unit is adapted to run the control algorithm, wherein the method includes the steps of:

performing a set of primary test functions by the secondary processing unit;

comparing a primary output of the primary processing unit after the control algorithm has been run and a test output of the secondary processing units;

responsively detecting a fault in the primary processing unit; and,

performing the first set of functions by the secondary processing unit upon detection of a fault in the primary processing unit.

5452. (Currently Amended). A method, as set forth in claim 51, wherein the primary processing unit controls ~~first system is~~ a brake system.

5553. (Currently Amended). A method, as set forth in claim 53 ~~51~~, wherein the primary processing unit controls ~~first system is~~ a steering system.

5654. (Currently Amended). A method ~~system~~, as set forth in claim 55 ~~53~~, wherein the steering system is a steer by wire system.

5755. (Currently Amended). A method ~~system~~, as set forth in claim 53 ~~51~~, wherein the primary processing unit controls ~~first system is~~ an engine control system.

5856. (Currently Amended). A method ~~system~~, as set forth in claim 53 ~~51~~, including the steps of:

performing a second set of functions by the secondary processing unit;

performing a set of secondary test functions by the primary processing unit; and,

wherein the secondary processing unit is adapted to perform a set of secondary test functions, and responsively detecting a fault in the secondary processing unit; and,

performing the second set of functions by the primary processing unit upon detection of a fault in the secondary processing unit.

57. (Cancelled).

58. (Cancelled).